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Total Number of Pages in This Submission

Application Number	09/940,709
Filing Date	August 28, 2001
First Named Inventor	Michael K. Gschwind
Art Unit	2186
Examiner Name	Woo H. Choi
Attorney Docket Number	YOR920010602US1 (8728-546)

ENCLOSURES *(Check all that apply)*

- [✔] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
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- [ ] CD, Number of CD(s) _____
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✔] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [✔] Other Enclosure(s) (please Identify below):

Transmittal of Appeal Brief

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	F. Chau & Associates, LLC		
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Printed name	Frank V. DeRosa		
Date	April 3, 2006	Reg. No.	43,584

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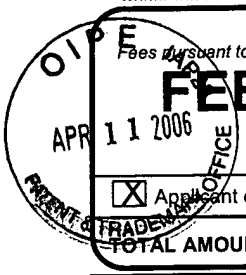

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL For FY 2005

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	09/940,709
Filing Date	August 28, 2001
First Named Inventor	Michael K. Gschwind
Examiner Name	Woo H. Choi
Art Unit	2186
Attorney Docket No.	8728-546

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	- 20 or HP =	Extra Claims	x Fee ($)	= Fee Paid ($)
_____		_____	25.00	0

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	- 3 or HP =	Extra Claims	x Fee ($)	= Fee Paid ($)
_____		0	200.00	0

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
360.00	0

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	- 100 =	Extra Sheets	/ 50 =	Number of each additional 50 or fraction thereof (round up to a whole number)	x Fee ($)	= Fee Paid ($)
_____		0		_____	250.00	0

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	0
Other: Appeal Brief Fee	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 43,584	Telephone 516-692-8888
Name (Print/Type)	Frank V. DeRosa		Date April 3, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPLICANT:	Michael Gschwind et al.	EXAMINER: Woo H. Choi
SERIAL NO.:	09/940,709	GROUP ART UNIT: 2186
FILED:	August 28, 2001	
FOR:	CONFIGURABLE MEMORY ARRAY	

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TRANSMITTAL OF APPEAL BRIEF

Sir:

Enclosed please find APPELLANTS' APPEAL BRIEF.

The amount of $500.00 is hereby authorized to be charged Deposit Account No. 50-0510/IBM (Yorktown Heights). Please charge any deficiency as well as any other fee(s) which may become due under 37 C.F.R. § 1.16 and/or 1.17, at any time during the pendency of this application, or credit any overpayment of such fee(s), to Deposit Account No. 50-0510/IBM (Yorktown Heights).

Respectfully submitted,

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Dated: April 3, 2006

Frank V. DeRosa

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants:	Gschwind, et al.	**Examiner:**	Choi, Woo H.
Serial No.:	09/940,709	**Group:**	Art Unit 2186
Filed:	August 28, 2001	**Docket No.:**	YOR920010602US1 (8728-546)

For: **CONFIGURABLE MEMORY ARRAY**

APPEAL BRIEF

Appeal from Group 2123

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I. INTRODUCTION

This Appeal is from a Final Office Action mailed on November 2, 2005 (hereinafter, referred to as the "Final Action") finally rejecting claims 1-8 and 10-37 of the above-identified application. The Appellants commenced this Appeal by a Notice of Appeal filed on February 3, 2006, and hereby submit this Appeal Brief in furtherance of the Appeal.

II. REAL PARTY IN INTEREST

The real party in interest for the above-identified application is International Business Machines Corporation, the assignee of the entire right, title and interest in and to the subject application by virtue of an assignment of recorded in the U.S. Patent and Trademark Office.

III. RELATED APPEALS AND INTERFERENCES

There are no Appeals or Interferences known to Applicant, Applicant's representatives or the Assignee, which would directly affect or be indirectly affected by or have a bearing on the Board's decision in the pending Appeal.

IV. STATUS OF CLAIMS

Claims 1-37 are pending, claims 1-8 and 10-37 stand rejected and are under appeal, and claim 9 is objected to as being dependent on a rejected base claim, but would be allowable if rewritten as suggested on page 9 of the Final Action. The claims are set forth in the attached Appendix. Claims 1, 22, 26, 29, 30 and 33 are independent claims, where claims 2-21 depend directly or indirectly from claim 1, claims 23-25 depend directly or indirectly from claim 26,

where claims 31-32 depend directly or indirectly from claim 30 and where claims 34-37 depend directly or indirectly from claim 33.

V. STATUS OF AMENDMENTS

No claim amendments have been filed or entered subsequent to the Final Action.

VI. SUMMARY OF CLAIMED SUBJECT MATTER

For purposes of illustration, the invention of claims 1, 22, 26, 29, 30 and 33, will be described with reference to the exemplary FIGs. and corresponding text of Appellants' Specification (hereinafter, Spec.), for example, but nothing herein shall be deemed as a limitation on the scope of the invention. In general, the claimed inventions are direct to systems and methods for implementing configurable memory systems in which memory can be configured for use suitable for a wide range of applications. For instance, FIG. 1 of Spec. illustrates an electronic device (100) having a reconfigurable memory (130) which can be selectively configured as a local main memory (FIG. 2) or as cache memory (e.g., L2 cache as in FIG. 3), for example, (see, generally e.g., Spec. p. 10, line 8 - p. 14, line 16).

Claim 1 recites:

> A memory system on a chip, comprising:
> a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory, wherein the configurable memory comprises a memory array in which both tag bits and data bits are stored in a single data line in the memory array, in the first mode of operation.

An exemplary embodiment of claim 1 may be described with reference to FIGs. 1 and 4 and relevant description in Spec. For example, FIGs. 1 and 4 generally depict a memory system (130) on a chip (100) having a configurable memory (130) having a first mode of operation wherein the configurable memory (130) is configured as a cache and a second mode of operation wherein the configurable memory (130) is configured as a local, non-cache memory (see, e.g., Spec. p. 14, line 18 ~ page 16, line 13). The configurable memory (130) comprises a memory array (410) (FIG. 4) The memory array (410) includes both tag bits and data bits are stored in a single data line in the memory array (410), in the first mode of operation (see, e.g., Spec. p. 18, 10-14).

Claim 22 recites:

> A memory system on a chip, comprising:
> a configurable Random Access Memory (RAM) array having a first mode of operation wherein the configurable RAM array is configured as a local, non-cache memory and a second mode of operation wherein the configurable RAM array is configured as a cache,
> wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

An exemplary embodiment of claim 22 may be described with reference to FIGs. 1 and 4 and relevant description in Spec. For example, FIGs. 1 and 4 generally depict a memory system (130) on a chip (100) having a configurable RAM array (410) having a first mode of operation wherein the configurable RAM array (410) is configured as a local, non-cache memory and a second mode of operation wherein the configurable RAM array is configured as a cache (see, e.g., Spec. p. 14, line 18 ~ page 16, line 13; p. 5, lines 5-15). The first mode of operation or the

second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register (see, e.g., Spec., p. 15, lines 8-14, FIG. 4, element (420); and FIG. 5 (steps 550, 550a); p. 23, lines 3-17).

Claim 26 recites:

> A data storage system, comprising:
> at least one microprocessor; and
> a configurable memory, integrated with the at least one processor, for servicing the at least one microprocessor in a first mode of operation that emulates a local, non-cache memory and a second mode of operation that emulates a cache,
> wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation, wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

An exemplary embodiment of claim 26 may be described with reference to FIGs. 1 and 4 and relevant description in Spec. For example, FIGs. 1 and 4 illustrate a data storage system, comprising at least one microprocessor (100), and a configurable memory (130), integrated with the at least one processor, for servicing the at least one microprocessor in a first mode of operation that emulates a local, non-cache memory and a second mode of operation that emulates a cache, wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation, wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register(see, e.g.,

Spec., p. 15, lines 8-14, FIG. 4, element (420); FIG. 5 (steps 550, 550a); p. 23, lines 3-17).

Claim 29 recites:

> A memory system on a chip, comprising:
> a processor; and
> a configurable memory having three modes of operation, a first mode of operation for emulating a local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of operation for emulating both the local memory and the cache, wherein any of the three modes of operation may be selected at any given time during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

An exemplary embodiment of claim 29 may be described with reference to FIGs. 1 and 4 and relevant description in Spec. For example, FIGs. 1 and 4 illustrate a memory system on a chip (100), comprising a processor (120); and a configurable memory (130) having three modes of operation, a first mode of operation for emulating a local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of operation for emulating both the local memory and the cache, wherein any of the three modes of operation may be selected at any given time during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register(see, e.g., Spec., p. 15, lines 8-14, FIG. 4, element (420); FIG. 5 (steps 550, 550a); p. 23, lines 3-17).

Claim 30 recites:

> A method for accessing data, comprising the steps of:
> providing a configurable memory on a chip;
> providing control logic on the chip for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;
> configuring the configurable memory as a local, non-cache memory in the first mode of operation;
> configuring the configurable memory as a cache in the second mode of operation; and
> accessing the data from the configurable memory, based upon a mode of the configurable memory,
> wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

An exemplary embodiment of the method of Claim 30 is illustrated in FIG. 6 and the corresponding description in Spec. In particular, FIG. 6 illustrates a method for accessing data, comprising the steps of providing a configurable memory on a chip (step 605), providing control logic on the chip for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation (step 610), configuring the configurable memory as a local, non-cache memory in the first mode of operation (step 680), configuring the configurable memory as a cache in the second mode of operation (step 685); and accessing the data from the configurable memory, based upon a mode of the configurable memory (step 690). (See, e.g., Spec., p. 24, line 14 ~ p. 26, line 2). The first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register (see, e.g., Spec. p. 23,

lines 3-17).

Claim 33 recites:

> A method for accessing data, comprising the steps of:
> providing a configurable memory in a package;
> providing control logic in the package for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;
> configuring the configurable memory as a local, non-cache memory in the first mode of operation;
> configuring the configurable memory as a cache in the second mode of operation, and
> accessing the data from the configurable memory, based upon a mode of the configurable memory,
> wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

An exemplary embodiment of the method of Claim 33 is illustrated in FIG. 6 and the corresponding description in Spec. In particular, FIG. 6 illustrates a method for accessing data, comprising the steps of providing a configurable memory in a package (step 650), providing control logic in the package for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation (step 655), configuring the configurable memory as a local, non-cache memory in the first mode of operation (step 680), configuring the configurable memory as a cache in the second mode of operation (step 685) and accessing the data from the configurable memory, based upon a mode of the configurable memory (step 690) (See, e.g., Spec., p. 24, line 14 ~ p. 26, line 2). The first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to

at least one address range contained in at least one configuration register (see, e.g., Spec. p. 23, lines 3-17).

VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-8, 10-20, 22, 23, 25-34 and 37 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,678,790 to Kumar.

B. Claims 1, 10-14 and 21 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,321,318 to Baltz.

C. Claim 24 stands rejected as being unpatentable over Kumar in view of U.S. Patent 6,377,912 to Sample, or in the alternative in view of U.S. Patent 6,611,796 to Natarajan.

D. Claims 34 and 35 stand rejected as being unpatentable over Kumar in view of U.S. Patent 6,426,549 to Isaak.

VIII. ARGUMENTS

A. The Teachings of Kumar Do Not Support the Anticipation Rejections

For a claim to be anticipated under 35 U.S.C. § 102, all elements of the claim must be found in a single prior art reference (see, e.g., Scripps Clinic & Research Found. v. Genentech Inc., 927 F.2d 1565, 1576, 18 U.S.P.Q.2d. 1001, 1010 (Fed. Cir. 1991)). The identical invention must be shown in as complete detail as is contained in the claim. (See MPEP § 2131). The single prior art reference must disclose all of the elements of the claimed invention functioning essentially in the same manner (see, e.g., Shanklin Corp. v. Springfield Photo Mount Corp, 521 F.2d 609 (1st Cir. 1975)).

Here, Applicants respectfully assert that Kumar is legally deficient to establish prima facie case of anticipation against any of claims 1-8, 10-20, 22, 23, 25-34 and 37. At the very least, Kumar does not anticipate independent claims 1, 22, 26, 29, 30 and 33 for the following reasons.

(i) Kumar Does Not Anticipate Claim 1

With regard to claim 1, Applicants respectfully assert that Kumar does not disclose, for example, a configurable memory having *a memory array in which **both** tag bits and data bits are stored in a single data line in the memory array in a first mode of operation where the configurable memory is configured as a cache*, as claimed in claim 1.

The rejection of claim 1 is based, in part, on the Examiner's finding that Kumar discloses a configurable memory having *"a memory array in which both tag bits (figure 2, 50) and data bits are stored in a single data line (col. 3, lines 32-33) in the memory array (figure 1, 12), in the second mode of operation."* (See, p. 2 of the Final Action). As can be readily gleaned from the Examiner's Response to Arguments on p. 9 of the Final Action, this finding is premised on the Examiner's finding that Kumar teaches *"forming a single logical data line in the memory array (12)"* based on Kumar's disclosure in Col. 3, lines 32-33 that each row of the tag array (50) corresponds to one of the data lines in the data array (52). From this, it appears that the Examiner determines that *"forming a single logical data line in the memory array (12)"* teaches a configurable memory array (12) that contains tag bits and data bits in the same array (12). This argument is not directly on point and is seemingly irrelevant to the specific claim language.

Indeed, even assuming that the Examiner's characterization of Kumar as teaching a "single logical data line" is correct, the Examiner offers no explanation as to how the "single

logical data line" is the same or similar to or otherwise anticipates the claim feature of *a memory array in which both tag bits and data bits are stored in a single data line in the memory array*, as in claim 1. Moreover, the Examiner's characterization of element (12) as being a memory array is seemingly incorrect as Kumar teaches a configurable memory system (12) having a plurality of separate memory arrays (50) and (52), for example. It should be noted that claim 1 recites a configurable memory that comprises a memory array, and it is the memory array that stores both the tag and data bits in a single data line when the memory is in cache mode.

Furthermore, the Examiner's finding squarely contradicts Kumar's clear teaching of a reconfigurable memory (12) having separate memory arrays – a tag array (50) and a cache data array (52), for cache operation (as depicted in FIG. 2). Indeed, Kumar clearly discloses that the data array (52) stores a data line and the tag array (50) stores sets of tags (Col. 3, lines 27-35). In other words, Kumar teaches that tag bits are not stored with data bits in a data line of a memory array configured as a cache (as in claim 1), but rather that data bits and tag bits are stored and accessed from different arrays. It should be noted that Applicants' Specification indicates that there is a difference between cache tags being stored in data lines stored in a memory array or having separate memory arrays for storing data and tags (see, Spec. page 18, lines 10-14).

Accordingly, in view of the above, the Examiner has not sufficiently demonstrated how Kumar discloses, for example, a configurable memory having *a memory array in which **both** tag bits and data bits are stored in a single data line in the memory array in a first mode of operation where the configurable memory is configured as a cache*, as claimed in claim 1. Therefore, at the very least, the Final Action fails to present a *prima facie* case of anticipation of claim 1 in view of Kumar.

(ii) Kumar Does Not Anticipate Claims 22, 26, 30 and 33

Claims 22, 26, 30 and 33 commonly recite the claim feature of *wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register,* which Applicants contend at the very least is one patentably distinguishing feature over Kumar. The rejection of claims 22, 26, 30 and 33 is based on the same common ground, and thus, these claims will be grouped together for purposes of this appeal. Indeed, the basis for Examiner's rejection of Claims 22, 26, 30 and 33 as set forth on page 3 of the Final Action is as follows:

> With respect to claims 22, 26, 30 and 33, the Examiner notes that each of the added limitations claims a capability to select the first mode or the second mode. The[y] do not require mode selection based on an address comparison. Kumar's memory supports mode selection. It is capable of supporting a mode selection based on an address comparison.

Clearly, this argument fails to support a *prima facie* case of anticipation. The Examiner seems to place no patentable weight on the claim limitation of "*wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register*" on the ground that it is only a "capability" and not "required". It seems that the Examiner's argument is based on the claim language "... can be selected ... " This argument is seemingly meritless.

Assuming that the Examiner's characterization of the claims as reciting only a capability

is correct, there is no legal or logical reason for Examiner's refusal to place patentable weight and consideration on a claim feature regarding a capability of a claimed device to perform a claimed function. Indeed, if a claimed device is capable of performing a claimed function, and that same claimed function is not supported or disclosed in the prior art, then the claim feature is a patentably distinguishing feature and should be considered.

It should be noted that the **MPEP Section 2173.05(h)** indicates that claim language such as "capable of" or "may be" are valid terminologies that can be used in proper context to define a particular capability or purpose that is served by a recited element or step. In the case at bar, the claimed feature in which a first or second mode *can be* selected based on comparing a supplied address to at least one address range contained in at least one configuration register, is a definite, patentably distinguishing feature of Kumar. It should be further noted that Applicants Specification teaches that the claimed devices and methods may implement mode configuration options either individually or in combination (see, e.g., Spec. p. 20, lines 12-15). This provides clear support for claim language that a mode selection *can be* performed by a particular method, but not required to be performed by such method.

Moreover, there is no support for the Examiner's assertion that Kumar teaches a memory system that is capable of supporting a mode selection based on an address comparison. The Examiner fails to point to any specific teaching in Kumar to support such finding. The reason is simple - Kumar does not disclose or suggest any such mode selection feature (see, e.g., Kumar, Col. 2, lines 47-60, where the disclosed mode selection options do not disclose or suggest the claimed mode selection features).

In fact, the Examiner has already acknowledged at the very least that the subject matter of

Claim 9 is not disclosed by any of the cited art of record. Claims 22, 26, 30 and 33 recite subject matter similar to that recited in claim 9. However, claim 9 recites that a .... mode ***is*** selected during the program execution ... , whereas claims 22, 26, 30 and 33 recite that a .... mode ***can be*** selected .... As explained above, however, the Examiner's characterization of "can be" as a hypothetical feature, distinguished from "is", is improper as a matter of law. Again, if a device is capable of performing a function, that function is a distinguishing feature. The Examiner's argument is seemingly premised on some theory that a "capability" is merely hypothetical and that since Kumar teaches mode selection, it is possible for Kumar to support mode selection based on address comparison, as recited in the claimed inventions. Clearly, there is error in this analysis and the Examiner's failure to consider the claimed features constitutes reversible error.

(iii) Kumar Does Not Anticipate Claim 29

Applicants respectfully assert that Kumar does not disclose or suggest, e.g., a memory system on a chip comprising a configurable memory having three modes of operation ... *wherein any of the three modes of operation may be selected at any given time during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register* , as recited in claim 29.

The basis for the Examiner's rejection of claim 29, as set forth on page 3 of the Final Action , is essentially that the claimed feature of *wherein any of the three modes of operation may be selected at any given time during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register*, is merely an "optional feature", which Examiner gives no patentable weight. The Examiner's failure to consider this feature is seemingly based on the language of "may be selected" similar to the

language "can be selected" in claims 22, 26, 30 and 31 as discussed above.

However, the Examiner's analysis is flawed for the same reasons explained above. Claim 29 recites a memory system having a configurable memory with three modes of operation, wherein any of the three modes may be selected based on address comparison..... . The mode selection feature of the claimed memory system is a definite and positive recitation of a claim feature that provides a patentable distinction over Kumar, and which should have been considered in Examiner's analysis. Again, although Kumar discloses mode selection, there is nothing in Kumar that discloses or suggests that mode selection may be performed by *comparing a supplied address to at least one address range contained in at least one configuration register.* Again, the Examiner's failure to consider the claimed features constitutes reversible error.

B The Teachings of Baltz Do Not Support the Anticipation Rejections

Applicants respectfully assert that Baltz is legally deficient to establish a *prima facie* case of anticipation against claims 1, 10-14 and 21. At the very least, Baltz does not disclose a configurable memory that comprises a memory array in which both tag bits and data bits are stored in a single data line in the memory array in a first mode of operation where the configurable memory is configured as a cache, as claimed in claim 1.

The basis for Examiner's rejection of claim 1 in view of Baltz is set forth on page 7 of the Final Action. The Examiner contends that FIG. 9, elements 30, 31 and 32 illustrate a memory array for storing tag bits and data bits in a single data line in the memory array. However, similar to those arguments presented above with regard to claim 1 in view of Kumar, Baltz teaches separate tag memories (33, 32) (FIG. 9) of a memory controller (30) that are distinct from the

memory data array (31) (see FIG. 1). Accordingly, for at least the above reasons, claim 1 is patentably distinct from Baltz. Claims 10-14 and 21 are patentable over Baltz at least by virtue of their dependence from claim 1.

It should be noted that claims 10-14 are further patentable over Baltz and Kumar for similar reasons discussed above. The Examiner's rejection of claims 10-14 is not based on cited art, but rather the Examiner's failure to consider and simply dismiss the claim language as being a capability. Thus for similar reasons given above, the Examiner's rejection of claims 10-14 constitutes reversible error.

C The Combination of Kumar and Sample or Natarajan is Legally Deficient to Establish a Prima Facie Case of Obviousness Against the Claimed Inventions

Applicants respectfully submit that the Examiner has not presented a prima facie case of obviousness against claim 24 based on the combination of Kumar and Sample, or Kumar and Natarajan. In rejecting claims under 35 U.S.C. 103, the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532 (Fed. Cir. 1993). The burden of presenting a prima facie case of obviousness is only satisfied by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988). The test for obviousness is what the combined teachings of the applied prior art references would have suggested to one of ordinary skill in the art. In re Keller, 642 F.2d 413, 435; 208 U.S.P.Q. 871, 881 (CCPA 1981). The suggestion to combine the references should come from the prior art, and the Examiner cannot use hindsight gleaned from

the invention itself to pick and choose among related prior art references to arrive at the claimed invention. In re Fine, 837 F.2d at 1075. If the Examiner fails to establish a prima facie case, the rejection is improper and must be overturned. In re Rijckaert, 9 F.3d at 1532 (citing In re Fine, 837 F.2d at 1074).

Rather than provide a detailed explanation as to the impropriety of such rejections, it is suffice to say that the obviousness rejections are invalid at least for the same reasons given above for claim 22. Indeed, because claim 24 incorporates the elements of claim 22 by virtue of dependency, and since the rejection of claim 22 is primarily based on an improper finding of Kumar anticipating claim 22, the Final Action fails at the very least to demonstrate how the combined teachings of Kumar and Sample or Natarajan meet the elements of claim 24. \

D The Combination of Kumar and Isaak is Legally Deficient to Establish a Prima Facie Case of Obviousness Against the Claimed Inventions

Applicants respectfully submit that the Examiner has not presented a prima facie case of obviousness against claims 34 and 35 based on the combination of Kumar and Isaak Again, rather than provide a detailed explanation as to the impropriety of such rejections, it is suffice to say that the obviousness rejections are invalid at least for the same reasons given above for claim 33. Indeed, because claims 34 and 35 incorporate the elements of claim 33 by virtue of dependency, and since the rejection of claim 33 is primarily based on an improper finding of Kumar anticipating claim 33, the Final Action fails at the very least to demonstrate how the combined teachings of Kumar and Isaak meet the elements of claims 34 and 35.

E. CONCLUSION

Accordingly, for at least the above reasons, it is respectfully requested that the Board reverse all claim rejections under 35 U.S.C. §§ 102 and 103.

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Claims Appendix

1. A memory system on a chip, comprising:

a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory, wherein the configurable memory comprises a memory array in which both tag bits and data bits are stored in a single data line in the memory array, in the first mode of operation.

2. The memory system of claim 1, wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by an other selection of an other of the first mode of operation and the second mode of operation.

3. The memory system of claim 1, wherein the first mode of operation or the second mode of operation is selected at the burn-in time.

4. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a power-up time.

5. The memory system of claim 4, wherein the first mode of operation or the second mode of operation is selected at the power-up time using an external signal

6. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected during a program execution.

7. The memory system of claim 6, wherein the first mode of operation or the second

mode of operation is selected during the program execution based upon a value of a special configuration register.

8. The memory system of claim 6, wherein the first mode of operation or the second mode of operation is selected during the program execution based upon a value of an external signal.

9. The memory system of claim 6, wherein the first mode of operation or the second mode of operation is selected during the program execution based upon comparing a supplied address to at least one address range contained in at least one configuration register.

10. The memory system of claim 1, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses.

11. The memory system of claim 10, wherein the range of addresses are determined at a burn-in time.

12. The memory system of claim 10, wherein the range of addresses are determined at a boot-up time.

13. The memory system of claim 10, wherein the range of addresses are determined dynamically.

14. The memory system of claim 10, further comprising a configuration register for storing the range of addresses.

15. The memory system of claim 1, wherein the configurable memory comprises:
memory configuration logic for selecting the first mode of operation or the second mode

of operation.

16. The memory system of claim 1, wherein the configurable memory is capable of selecting one of a local memory read mode and a local memory write mode in the first mode of operation and is further capable of selecting one of a cache read mode and a cache write mode in the second mode of operation.

17. The memory system of claim 2, wherein the selection may be overridden by the other selection dynamically.

18. The memory system of claim 1, wherein the configurable memory comprises a plurality of static random access memory cells.

19. (Original) The memory system of claim 1, wherein the configurable memory comprises a plurality of dynamic random access memory cells.

20. (Original) The memory system of claim 1, wherein the configurable memory is capable of being dynamically employed as a sole memory serving the processor and as a portion of a larger, memory hierarchy.

21. The memory system of claim 1, wherein the first mode of operation and the second mode of operation are employed concurrently.

22. A memory system on a chip, comprising:

a configurable Random Access Memory (RAM) array having a first mode of operation wherein the configurable RAM array is configured as a local, non-cache memory and a second mode of operation wherein the configurable RAM array is configured as a cache,

wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range

contained in at least one configuration register.

23. The memory system of claim 22, further comprising control logic for selectively providing direct access to the configurable RAM array as the local, non-cache memory in the first mode of operation and as the cache in the second mode of operation.

24. The memory system of claim 22, wherein a the single logical line spans several physical macro cells.

25. The memory system of claim 22, further comprising:

tag match logic for determining a match between the stored tag bits and bits corresponding to a memory access; and

at least one multiplexer for selecting and outputting data corresponding to the memory access, when the match is determined.

26. A data storage system, comprising:

at least one microprocessor; and

a configurable memory, integrated with the at least one processor, for servicing the at least one microprocessor in a first mode of operation that emulates a local, non-cache memory and a second mode of operation that emulates a cache,

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation, wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

27. The data system of claim 26, wherein the at least one microprocessor and the configurable memory array are integrated on a single chip.

28. The data system of claim 26, wherein the at least one microprocessor and the configurable memory array are integrated in a single package.

29. A memory system on a chip, comprising:

a processor; and

a configurable memory having three modes of operation, a first mode of operation for emulating a local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of operation for emulating both the local memory and the cache,

wherein any of the three modes of operation may be selected at any given time during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

30. A method for accessing data, comprising the steps of:

providing a configurable memory on a chip;

providing control logic on the chip for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;

configuring the configurable memory as a local, non-cache memory in the first mode of operation;

configuring the configurable memory as a cache in the second mode of operation, wherein the configurable memory comprises a memory portion for storing tag bits and data bits in a single data line in the memory portion, in the second or third mode of operation; and

accessing the data from the configurable memory, based upon a mode of the configurable memory,

wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

31. The method of claim 30, further comprising the steps of:

providing at least one microprocessor for servicing memory access instructions for the configurable memory; and

integrating the at least one microprocessor with the configurable memory on the chip.

32. The method of claim 30, wherein the chip comprises a single chip.

33. A method for accessing data, comprising the steps of:

providing a configurable memory in a package;

providing control logic in the package for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation;

configuring the configurable memory as a local, non-cache memory in the first mode of operation;

configuring the configurable memory as a cache in the second mode of operation, wherein the configurable memory comprises a memory portion for storing tag bits and data bits in a single data line in the memory portion, in the second mode of operation; and

accessing the data from the configurable memory, based upon a mode of the configurable memory,

wherein the first mode of operation or the second mode of operation can be selected during a program execution based on comparing a supplied address to at least one address range contained in at least one configuration register.

34. The method of claim 33, further comprising the steps of:

providing at least one microprocessor for servicing memory access instructions for the configurable memory; and

integrating the at least one microprocessor with the configurable memory in the package.

35. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a chip stack technique.

36. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a flip chip technique.

37. The method of claim 34, wherein said integrating step integrates the at least one microprocessor with the configurable memory based upon a multi-chip module.

Evidence Appendix

There is no evidence submitted pursuant to 37 CFR §§ 1.130, 1.131 or 1.132 or any other evidence entered by the examiner and relied upon by appellant in this Appeal.

Related Proceedings Appendix

None.